Amendments to the Specification:

Enclosed is a Substitute Specification and a corresponding marked-up copy showing the changes made to the specification. No new matter has been added.

CLEAN COPY OF SPECIFICATION 09/801,637

INTERLEAVER MEMORY ACCESS APPARATUS AND METHOD OF CDMA SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a CDMA system, and more particularly to an interleaver memory access apparatus and method of a CDMA system.

2. Description of the Background Art

Figure 1 is a schematic block diagram of a general CDMA system in accordance with a conventional art. As shown in the drawing, the conventional CDMA system includes a frame quality indicator 10 for attaching a frame quality indicator indicating a data rate to a source data, a trail bit attaching unit 20 for attaching an 8 bit encoder trail bit to an output of the frame quality indicator 10, a convolutional encoder 30 for receiving the data bit from the trail bit attaching unit 20 and generating three code symbols (a serial data) per each data bit, a code symbol repeating unit 40 for repeating a symbol for the convolutional encoder 30 to make the same data size as the full rate, an interleaver memory 50 for storing the code symbols outputted from the code symbol repeating unit 40 according to row and column addresses outputted from an address generator 60, an orthogonal modulator 70 for receiving the code symbols from the interleaver memory 50, generating one Walsh index for 6 bit code symbols and outputting 64 bit Walsh codes, and a radio frequency processor 80 for spread-modulating the 64 bit Walsh chips outputted from the orthogonal modulator 70 and transmitting a radio frequency signal.

The operation of the CDMA system constructed as described above will now be explained. For explanation's sake, it is assumed that the data rate is 4800bps.

When a source data, such as an analog voice signal, is inputted to the CDMA system, the inputted source data is PCM-modulated and inputted through a VOCODER (not shown) to the frame quality indicator (FQI) 10.

Then, the frame quality indicator 10 attaches a predetermined bit of a frame quality indicator indicating 4800bps to the inputted source data and outputs a 4.4kbps data bits. The trail bit attaching unit 20 attaches 8 bits of encoder trail bits to the 4.4kbps data bits and outputs 4.8kbps data bits.

The convolutional encoder 30 generates three code symbols for each data bit outputted from the trail bit attaching unit 20 and outputs a 14.4ksps code symbol.

The code symbol repeating unit 40 repeatedly outputs by one time the code symbols inputted from the convolutional encoder 30 (e.g., each code symbol is output twice such that the code symbols are repeated once) and generates a 28.8ksps code symbol, to make the same data size as that of the full rate (9600bps).

When the data rate is 2400bps, the code symbol repeating unit 40 repeats the code symbols 3 times (e.g., each code symbol is output four times such that the code symbols are repeated three times). When the data rate is 1200bps, the code symbol repeating unit 40 repeats the code symbols 7 times (e.g., each code symbol is output eight times - the first code symbol is output and then repeated seven times). Thus, the rate of the code symbols outputted from the code symbol repeating unit 40 has the same data size as that of the full rate.

As shown in Figure 2, the interleaver memory 50 includes 32 rows and 18 columns and writes and reads the code symbols outputted from the code symbol

repeating unit 40 according to the row and the column address outputted from the address generator 60.

The orthogonal modulator 70 decodes the code symbols, which are inputted from the interleaver memory 50, by six codes to generate one Walsh index, and selectively outputs one of the 64 bit Walsh codes using the generated Walsh index. Therefore, the ratio frequency processor 80 spread-modulates the 4.8Ksps Walsh chips outputted from the orthogonal modulator 70 and converts it to a radio frequency signal and transmits the converted radio frequency signal.

The access operation of the interleaver memory 50 will now be described in detail.

Generally, the CDMA system supports a variable data rate. Accordingly, the code symbol repeating unit 40 repeats the code symbols (the serial data) for the data rates except for the full rate (9600bps), that is, a half rate (4800bps), a quarter rate (2400bps) and an eighth rate (1200bps), to process easily the data.

The CDMA system transmits a data through a radio interface. However, when a data is transmitted through the radio interface, a data loss (an error) may unexpectedly occur due to various noise. Thus, before modulating and transmitting of the code symbol, a data interleaving is performed to prevent a burst error.

In the conventional CDMA system, the data interleaving is implemented by the interleaver memory 50 and the address generator 60 shown in Figure 1.

The interleaver memory 50 sequentially writes the code symbols outputted from the code symbol repeating unit 40 at the position of a normal interleaver memory map as shown in Figure 2 according to the row and the column addresses outputted from the address generator 60. Consequently, 1~576 code symbols (one frame data) are written in the interleaver memory 50.

Figure 3 illustrates an example of an interleaver memory map for each data rate.

Once the data writing operation is completed, the reading operation of the interleaver memory 50 is performed according to the order determined in a CDMA mobile communication standard; that is, according to the order of the following row address in the normal interleaver memory map of Figure 2.

Full rate: 1 2 3 4 5 6 7 8 9 10 .... 25 26 27 28 29 30 31 32

Half rate 1 3 2 4 5 7 6 8 9 11 .... 25 27 26 28 29 31 30 32

Quarter rate: 1 5 2 6 3 7 4 8 .... 25 29 26 30 27 31 28 32

Eighth rate: 1 9 2 10 3 11 4 12 .... 21 29 22 30 23 31 24 32

For example, assuming the code symbols of the full rate are stored in the interleaver memory 50 in the form as shown in Figure 4, the address generator 60 changes the column from 1~12 in a state that it has outputted one row address, so that the 12 bit code symbols are sequentially read from the interleaver memory 50 as shown in Figure 5.

Code symbols of other data rates are also read according to the same row address and the column address order as that of the full rate.

As described above, in the conventional CDMA system, the access (the reading and writing) operation of the interleaver memory is repeatedly performed by code symbols.

In this respect, however, in order to read and write the code symbols of one frame, the serial data, since the address (the row and the column) generation and the access operation of the interleaver memory should be performed so frequently, causing a disturbance to the rapid data processing and a low power consumption.

In addition, in the conventional CDMA system, the orthogonal modulator 70 receives 6 code symbols, the serial data to generate one Walsh index. However, in order to generate one Walsh index, the orthogonal modulator 70 should wait for 6 bit code symbols to be received from the interleaver memory 50, causing a problem that the data processing time is increasingly extended.

Thus, the conventional CDMA system fails to cope suitably with the rapid data processing and the minimum power consumption required for the mobile communication system.

SUMMARY OF THE INVENTION

Therefore, an object of the present invention is to provide an access apparatus of an interleaver memory that is capable of reducing a power consumption and increasing a data access speed by improving the addressing and access operation of an interleaver memory, and its method.

Another object of the present invention is to provide an access apparatus of an interleaver memory that is capable of increasing a data processing rate by receiving 6 code symbols in parallel and generating one Walsh index, and its method.

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described herein, there is provided an interleaver memory access apparatus of a CDMA system including: an interleaver memory for storing code symbols to be transmitted; a shift register unit for simultaneously receiving 18 bit code symbols from the interleaver memory and outputting it by 6 code symbols; an index decoding unit for decoding the 6 code symbols outputted from the shift register unit and generating a Walsh index; an address generator and control logic for controlling the access operation of the

interleaver memory and the input and output operation of the shift register unit and the index decoding unit; and an orthogonal modulator for outputting 64 Walsh codes on the basis of the Walsh index outputted from the index decoding unit.

To achieve the above objects, there is also provided an interleaver memory access method of a CDMA system including: storing code symbols to be transmitted in the interleaver memory; reading 1-row code symbols stored in the interleaver memory by using a row address signal and outputting them to the shift register unit; repeatedly accessing the first code symbols stored in the shift register unit according to the transfer rate of the code symbols; and decoding the 6 code symbols outputted from the shift register unit and generating one Walsh index.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

In the drawings:

Figure 1 is a schematic block diagram of a general CDMA system in accordance with a conventional art;

Figure 2 illustrates a normal interleaver memory map of Figure 1 in accordance with the conventional art;

Figure 3 illustrates an example of an interleaver memory map for each data rate in accordance with the conventional art;

Figure 4 illustrates an example of an interleaver memory map storing code symbols of a full rate in accordance with the conventional art;

Figure 5 illustrates addressing in the interleaver memory of Figure 4 and the corresponding data output values in accordance with the conventional art;

Figure 6 is a schematic block diagram of an interleaver memory access apparatus of a CDMA system in accordance with the present invention;

Figure 7 illustrates addressing and corresponding data output values of the interleaver memory of Figure 6 in accordance with the present invention;

Figure 8 illustrates an interleaver memory map storing code symbols of a half rate of Figure 6 in accordance with the present invention; and

Figure 9 illustrates addressing and corresponding data output values of the interleaver memory of Figure 8 in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

Figure 6 is a schematic block diagram of an interleaver memory access apparatus of a CDMA system in accordance with the present invention.

As shown in the drawing, the interleaver memory access apparatus of a CDMA system of the present invention includes an interleaver memory 100, a shift register unit 101 for simultaneously receiving 18 bit code symbols from the interleaver memory 100 and outputting three sets of 6 bit code symbols; an index decoding unit 102 for decoding the 6 bit code symbols outputted from the shift register unit 101 and

generating a Walsh index; an orthogonal modulator 103 for outputting 64 bit Walsh codes on the basis of the Walsh index outputted from the index decoding unit 102; and an address generator and control logic 104 for controlling the access operation of the interleaver memory 100 and the input and output operation of the shift register unit 101 and the index coding unit 102.

The interleaver memory 100 is constructed as a memory bank of the same size (576 bit) as that of the conventional art.

The shift register unit 101 includes two shift registers connected in series so that while one shift register performs a reading operation, the other one may perform a writing operation. Each shift register is divided into three storing regions and sequentially outputs 6 bit code symbols according to a data select signal (DS) outputted from the address generator and control logic (104).

The index decoding unit 102 includes first through third index decoders 50~52 which sequentially receive the 6 code symbols from each register of the shift register unit 101 and generate one Walsh index. The first through the third index decoders 50~52 are activated according to an enable signal (EN) outputted from the address generator and control logic 104.

The orthogonal modulator 103 generates only a Walsh code according to the Walsh index outputted from the index decoding unit 102, rather than generating both the Walsh index and the Walsh code as in the conventional art.

The operation of the interleaver memory access apparatus of the present invention constructed as described above will now be explained.

First, the access operation of the interleaver memory 100 is the same as that of the conventional art, except for the reading operation.

That is, in the present invention, when the reading operation of the interleaver memory is performed according to the order determined by the CDMA mobile communication standard, the column address is not used and only the row address is used.

Therefore, whenever a row address is inputted by the address generator and control logic 104, 1-row data (i.e., a single row) written in the interleaver memory 100, that is, 18 bit code symbols of Figure 2 are simultaneously read.

For example, assuming the code symbols of the full rate are stored in the interleaver memory 100 in the form of Figure 4, the interleaver memory 100 outputs one row of code symbols once according to the row addresses (1, ..., 16) sequentially inputted from the address generator and control logic 104 as shown in Figure 7. That is, the row address serves as a transmission signal of the symbol code.

Meanwhile, assuming the code symbols of a half rate are stored in the interleaver memory 100 in the form as shown in Figure 8, the interleaver memory 100 outputs one row of code symbols once according to the row addresses (1 3 5 7 9 11 13 15) inputted from the address generator and control logic 104. The code symbols stored in the even rows of the interleaver memory 100 are the code symbols which have been repeatedly stored in the symbol repeating unit of the conventional art, the same as the code symbols of the previous row, to facilitate data processing.

Accordingly, as shown in Figure 9, the code symbols stored in the even row of the interleaver memory 100 are not read from the interleaver memory 100, and the data select signal DS is outputted to repeatedly access the code symbols of the previous row which has been already transmitted to the shift register unit 101. This replaces the access operation of the code symbols stored in the even rows.

The first through the third index decoders 50~52 of the index decoding unit 102 are sequentially activated according to the enable signal EN outputted from the address generator and control logic 104, decode the 6 bit code symbols inputted from the shift register unit 101 and generate one Walsh index, respectively.

Accordingly, the orthogonal modulator 103 generates 64 bit Walsh codes according to the Walsh index outputted from the first through the third index decoders 50~52 and outputs them.

As so far described, according to the interleaver memory access apparatus and method of the CDMA system of the present invention, the interleaver memory performs reading operation by only using the row address. Consequently, a simple addressing is implemented for the memory access, so that the performance of the overall CDMA system as well as the data access speed can be enhanced.

In addition, since the code symbols of the previous row stored in the shift register are repeatedly accessed to be generated, rather than reading the repeated data stored in the interleaver memory. Consequently, the access number of the interleaver memory is considerably reduced, so that the power consumption is accordingly reduced for the memory access.

The present invention is also featured in that the Walsh index generation function, which is included in the orthogonal modulator of the conventional art, is separated therefrom, for which, instead, an index decoding unit is provided.

Moreover, since the 6 bit code symbols are simultaneously outputted from the shift register unit by using the one clock enable signal, the index decoding unit does not wait until the 6 bit code symbols are inputted as in the conventional art and can quickly generate the Walsh index. Thus, the operation speed of the orthogonal modulator can be remarkably improved.

As the present invention may be embodied in several forms without departing from the spirit or essential characteristics thereof, it should also be understood that the above-described embodiments are not limited by any of the details of the foregoing description, unless otherwise specified, but rather should be construed broadly within its spirit and scope as defined in the appended claims, and therefore all changes and modifications that fall within the meets and bounds of the claims, or equivalence of such meets and bounds are therefore intended to be embraced by the appended claims.